PVP 14

Code: EE5T6

III B.Tech - I Semester – Regular/Supplementary Examinations
October 2019

LINEAR AND DIGITAL INTEGRATED CIRCUIT APPLICATIONS

(ELECTRICAL & ELECTRONICS ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11 x 2 = 22 M

1.

a) Draw the block diagram of op-amp.
b) Define common mode voltage and differential mode voltage of op-amp.
c) Differentiate between active and passive filters.
d) Draw logarithmic amplifier circuit.
e) Explain the pin diagram of 555 timer.
f) Draw the block diagram of PLL.
g) Explain the operation of 2:1 multiplexer.
h) Design half adder and half subtractor.
i) Explain J-K flipflop excitation table.
j) Convert J-k flipflop to D flip-flop.
k) Explain slew rate of an op-amp.

PART – B

Answer any *THREE* questions. All questions carry equal marks.
3 x 16 = 48 M

2. a) Explain the operation of inverting and non-inverting amplifiers using op-amp with necessary equations. 8 M

b) Design the op-amp circuit which can give the output as $V_O=2V_1-3V_2+4V_3-5V_4$. 8 M

3. a) Draw the circuit of an Astable multivibrator using op-amp and derive the expression for its frequency of oscillations. 8 M

b) Design a second order low-pass Butterworth filter with a cut-off frequency of 12 KHz. 8 M

4. a) Discuss with relevant circuits and waveforms the working of Monostable multivibrator using 555 timer. 8 M

b) Draw the block diagram of a 565 PLL IC and explain its working. 8 M

5. a) Design 8:1 multiplexer by cascading 4:1 multiplexer. 8 M

b) Design a code converter that converts decimal digit to BCD. 8 M

6. a) Explain in detail about shift registers. 8 M

b) Design and explain a 4-bit ring counter using D-flip. 8 M